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EXAMINER	
BODDIE, WILLIAM	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,117	CHEN ET AL.	
	Examiner	Art Unit	
	William Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *7,11 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 7, 11 and 18 are objected to because of the following informalities: Claim 7 recites said "second scan lone", it appears Applicant intended this to read –scan line-. Claim 11 states "with one of scan lines of said active matrix", this is grammatically incorrect. One means of correction is –with one of a plurality of scan lines of said active matrix--. Claim 18 states "receiving a driving signal from preceding sub-circuit." Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 states that the second sub-circuit outputs the amplified driving signal via "said first output terminal." Currently the only "first output terminal" described is located in the *first* sub-circuit. It appears the Applicant intended for the second sub-circuit to output the amplified driving signal via a third output terminal, that is analogous to the first output terminal of the first sub-circuit.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 7-8, 11-14 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (current applicant; hereinafter APA) in view of Kubota et al. (US 6,580,411).

With respect to claim 1, APA discloses, a scan driving circuit (11 in fig .1) for use in a planar display comprising an active matrix (fig. 1), said scan driving circuit comprising:

a first sub-circuit (DC2 in fig. 1) receiving a driving signal (bottom input into A2 in fig. 1) and outputting said driving signal to a first scan line of said active matrix via a first output terminal after a predetermined time delay (bottom of para. 3); and

a second sub-circuit (DC3 in fig. 1) electrically connected to said first sub-circuit, receiving said driving signal transferred from a second output terminal of said first sub-circuit (note the wiring from DC2 to DC3), and outputting said driving signal to a second scan line of said active matrix after said predetermined time delay (para. 3).

APA does not expressly disclose, outputting a driving signal after a predetermined time delay or a unidirectional conducting device.

Kubota discloses, a first sub-circuit (LS_SR (n1), gl1 in fig. 31) and a second sub-circuit (LS_SR (n2), gl2 in fig. 31), wherein a driving signal (in and /in in fig. 23-24g) is output (out and /out in fig. 23-24g) after a predetermined time delay (note the delay in the two control signals fig. 24bc to fig. 24fg). Kubota further discloses, a unidirectional

conducting device (set of inverters in gl1 in fig. 31) electrically connected between said first output terminal (/n1 in fig. 31) and said second output terminal (gl1 in fig. 31).

Kubota and APA are analogous art because they are both from the same field of endeavor namely matrix display gate driver control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to insert the circuitry for the unidirectional conducting device, taught by Kubota, in the vertical scan driving circuitry of APA.

The motivation for doing so would have been to further amplify the driving signals prior to applying them to the gate lines (Kubota; col. 38, lines 25-27).

Therefore it would have been obvious to combine Kubota with APA for the benefit of signal amplification to obtain the invention as specified in claim 1.

With respect to claim 2, Kubota and APA disclose, the scan driving circuit according to claim 1 (see above).

APA further discloses, wherein said first sub-circuit (DC2 in fig. 1) comprises:

a shift register (A2 in fig. 1) receiving said driving signal and outputting said driving signal after said predetermined time delay in response to a clock signal (para. 3); and

a buffer circuit (B2 in fig. 1) electrically connected to said shift register (A2), said active matrix (10) and said second sub-circuit (DC3), amplifying power of said driving signal, and outputting said amplified driving signal to said active matrix and said second sub-circuit via said first output terminal and said second output terminal respectively (fig. 1 and para. 3).

With respect to claim 3, Kubota and APA disclose, the scan driving circuit according to claim 2 (see above).

APA further discloses, wherein said first sub-circuit (DC2 in fig. 1) further comprises an electro-static discharge protection circuit (C2 in fig. 1) electrically connected to said first output terminal of said buffer circuit (B2) for protecting said scan driving circuit from electro-static discharge damage (para. 3).

With respect to claim 7, Kubota and APA disclose, the scan driving circuit according to claim 2 (see above), wherein said second sub-circuit (DC3) comprises:

a shift register (A3 in fig. 1) electrically connected to said first sub-circuit (DC2), receiving said driving signal transferred from said second output terminal of said first sub-circuit, and outputting said driving signal after said predetermined time delay in response to said clock signal (para. 3);

a buffer circuit (B3 in fig. 1) electrically connected to said shift register (A3), said active matrix (10) and said second sub-circuit, amplifying power of said driving signal, and outputting said amplified driving signal to said second scan line of said active matrix via said first output terminal (fig. 1 and para. 3).

With respect to claim 8, Kubota and APA disclose the scan driving circuit according to claim 7 (see above). As the additional limitations of claim 8 are identical to claim 3, claim 8 is rejected on the merits shown above in claim 3.

With respect to claim 11, APA discloses, a scan driving circuit (11 in fig. 1) for driving an active matrix of a planar display (10 in fig. 1), said driving circuit comprising a

plurality of sub-circuits (DC3-DC1) each in communication with one of scan lines of said active matrix, one of said sub-circuits comprising:

a signal receiving device (A3) for receiving a driving signal from preceding sub-circuit (para. 3);

a signal amplifying device (B2) for amplifying power of said driving signal and outputting an amplified driving signal (para. 3);

a second output terminal (see cascaded signal from previous sub-circuits in fig. 1) electrically connected to said signal amplifying device and next sub-circuit for transferring said amplified driving signal to said next circuit (para. 3).

APA does not expressly disclose, a unidirectional conducting device disposed downstream of said signal amplifying device for transferring said amplified driving signal to said one of said scan lines unidirectionally via a first output terminal.

Kubota discloses, a unidirectional conducting device (set of inverters in gl1 in fig. 31) electrically connected between a first output terminal (gl1 in fig. 31) and a second output terminal (/n1 in fig. 31).

Kubota and APA are analogous art because they are both from the same field of endeavor namely matrix display gate driver control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to insert the circuitry for the unidirectional conducting device, taught by Kubota, in the vertical scan driving circuitry of APA.

The motivation for doing so would have been to further amplify the driving signals prior to applying them to the gate lines (Kubota; col. 38, lines 25-27).

Therefore it would have been obvious to combine Kubota with APA for the benefit of signal amplification to obtain the invention as specified in claim 11.

With respect to claim 12, Kubota and APA disclose, the scan driving circuit according to claim 11 (see above).

APA further discloses, wherein said signal receiving device is a shift register (A3 in fig. 1).

With respect to claim 13, Kubota and APA disclose, the scan driving circuit according to claim 11 (see above).

Kubota further discloses, wherein said driving signal received by said signal receiving device is transferred to said signal amplifying device after a predetermined time delay in response to a clock signal (note the delay in the two control signals fig. 24bc to fig. 24fg; also note the input clock signals into the shift registers of APA).

With respect to claim 14, Kubota and APA disclose, the scan driving circuit according to claim 11 (see above).

APA further discloses, wherein said signal amplifying device is a buffer circuit (B3 in fig. 1).

Kubota further discloses, wherein said unidirectional conducting device is included in a buffer circuit (col. 38, lines 24-26).

With respect to claim 17, Kubota and APA disclose, the scan driving circuit according to claim 11 (see above).

APA further discloses, further comprising an electro-static discharge protection circuit (C2 in fig. 1) electrically connected to said sub-circuit (A2-B2 in fig. 1) and said

one of said scan lines for protecting said scan driving circuit from electro-static discharge damage (para. 3).

With respect to claim 18, APA discloses, a scan driving circuit (11 in fig. 1) for driving an active matrix of a planar display (10 in fig. 1), said driving circuit comprising a plurality of sub-circuits (DC3-DC1) each in communication with one of scan lines of said active matrix, one of said sub-circuits comprising:

a signal receiving device (A3) for receiving a driving signal from preceding sub-circuit (para. 3);

a buffer circuit comprising a signal amplifying device (B2) for amplifying power of said driving signal to output an amplified driving signal (para. 3);

an output terminal (see cascaded signal from previous sub-circuits in fig. 1) electrically connected to said signal amplifying device and next sub-circuit for transferring said amplified driving signal to said next circuit (para. 3).

APA does not expressly disclose, a unidirectional conducting device disposed downstream of said signal amplifying device for transferring said amplified driving signal to said one of said scan lines unidirectionally via a first output terminal.

Kubota discloses, a unidirectional conducting device (set of inverters in gl1 in fig. 31) electrically connected between a first output terminal (/n1 in fig. 31) and a second output terminal (gl1 in fig. 31).

For analogous art, combination and motivation see that above rejections of claims 1 and 11.

With respect to claim 19, Kubota and APA disclose, the scan driving circuit according to claim 18 (see above).

APA further discloses, wherein said signal receiving device is a shift register (A3 in fig. 1).

With respect to claim 20, Kubota and APA disclose, the scan driving circuit according to claim 18 (see above).

Kubota further discloses, wherein said driving signal received by said signal receiving device is transferred to said signal amplifying device after a predetermined time delay in response to a clock signal (note the delay in the two control signals fig. 24bc to fig. 24fg; also note the input clock signals into the shift registers of APA).

6. Claims 4-6, 9-10 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (current applicant; hereinafter APA) in view of Kubota et al. (US 6,580,411) and further in view of Asada (US 5,194,853).

With respect to claim 4, Kubota and APA disclose, the scan driving circuit according to claim 2 (see above).

Neither Kubota nor APA expressly disclose, wherein said buffer circuit comprises a plurality of NOT gates arranged in series.

Asada discloses, wherein a sub-circuit (101-108 in fig. 1) comprises a buffer circuit (104 in fig. 1) comprises a plurality of NOT gates arranged in series.

Asada, Kubota and APA are all analogous art because they are from the same field of endeavor namely, matrix display gate driver control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the buffer circuit of Kubota and APA with the series of NOT gates taught by Asada.

The motivation for doing so would have been to ensure proper signal propagation to the subsequent stage and stable execution of the shift register.

Therefore it would have been obvious to combine Asada with Kubota and APA for the benefit of reliable circuit behavior to obtain the invention as specified in claim 4.

With respect to claim 5, Asada, Kubota and APA disclose, the scan driving circuit according to claim 4 (see above).

Kubota further discloses, wherein said buffer circuit comprises at least a NOT gate (three inverters in fig. 31) electrically connected between said first output terminal (/n1 output down onto gl1 in fig. 31) and said second output terminal (/n1 line into 2nd LS_SR) in series functioning as said unidirectional conducting device (behavior of the NOT gate as a unidirectional conducting device is seen as inherent).

With respect to claim 6, Asada, Kubota and APA disclose, the scan driving circuit according to claim 5 (see above).

APA further discloses, wherein said NOT gates is one selected from a group consisting of an NMOS NOT gate, a PMOS NOT gate, and a CMOS NOT gate (para. 2).

With respect to claims 9-10, Kubota and APA disclose the scan driving circuit according to claim 7 (see above). As the additional limitations of claims 9-10 are

identical to those recited in claims 4 and 6, claims 9-10 are rejected on the same merits as shown above in claims 4 and 6.

With respect to claim 15, Kubota and APA disclose, the scan driving circuit according to claim 11 (see above).

Kubota further discloses, wherein said unidirectional conducting device comprises at least a NOT gate (three inverters in fig. 31) electrically connected between said first output terminal (/n1 output down onto gl1 in fig. 31) and said second output terminal (/n1 line into 2nd LS_SR) in series.

Neither Kubota nor APA expressly discloses, wherein said signal amplifying device comprises a plurality of NOT gates arranged in series.

Asada discloses, wherein a sub-circuit (101-108 in fig. 1) comprises a signal amplifying device (104 in fig. 1) that comprises a plurality of NOT gates arranged in series.

Asada, Kubota and APA are all analogous art because they are from the same field of endeavor namely, matrix display gate driver control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the buffer circuit of Kubota and APA with the series of NOT gates taught by Asada.

The motivation for doing so would have been to ensure proper signal propagation to the subsequent stage and stable execution of the shift register.

Therefore it would have been obvious to combine Asada with Kubota and APA for the benefit of reliable circuit behavior to obtain the invention as specified in claim 4.

With respect to claim 16, Asada, Kubota and APA disclose, the scan driving circuit according to claim 15 (see above).

APA further discloses, wherein said NOT gates are selected from a group consisting of an NMOS NOT gate, a PMOS NOT gate, and a CMOS NOT gate (para. 2).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AMR A. AWAD
PRIMARY EXAMINER

Wlb
5/8/06